TEMIC

Digital Integration

Design done by Customer

Introduction

When integrating the digital part of modern electronic system, various technical and financial criteria are considered.

Over 10 years of ASIC experience have shown that no methodology can meet them all in the same time. TEMIC experience at proposing its customers the most appropriate solution has become an art, resulting in long-term partnership.

Our customers/partners have themselves experienced several ways of doing ASICs, from the use of heavy internal investment with their own design centers, to the full sub-contracting to ASIC vendors from mere product specifications.

Know-how protection, engineering workload management and evolution of merchant CAD tools have been leader factors in the evolution of the preferred solutions.

The border between the own skills of equipment manufacturers and those of semiconductors makers has evolved : high level behavioral description -such as VHDL - has become the most appropriate language for users to bridge between system description and physical implementation.

On the other end, submicron electronics and faster digital systems have revealed new challenges to cope with the electrical behavior of signals, both on and outside the chip. For instance, clock or signal skews, cross-talks, noise, electromagnetic emission or susceptibility have become the main drivers of first-pass yields in design.

Testing of largely integrated systems -sometimes including processor cores- is also a matter of many trade-offs between circuit cost, development time and safety operation.

New generations of programmable devices such as CPLD or FPGA have also appeared, offering unbeatable flexibility and development time, but with many drawbacks in cost, sourcing , logistics, reliability, etc.

On top of the long experince of our designers, TEMIC has developed an unmatched choice of ASIC solutions offering the best trade-off in development or production cost, flexibility or performance.

Our solutions are also compatible with previous choices or vendor policies from our clients. On top of our proven capacity to deliver high-quality silicon devices in volume, we are recognized for helping them to find the way to secure their present or future supplies, while remaining competitive along the lifetime of their systems.

TEMIC is committed to help its clients to save time, money, while avoiding thrilling hassle.

Digital Integration

Design done by Customer

Introduction

Design is fully done by Customer from specification to final postlayout simulation. Design Rule Check and Layout Versus Schematic are performed by Customer under its responsibility, except specific agreement. Test vectors if applicable are delivered by customer according to MHS rules.

CB6 0.6µm CMOS Cell-Based Designs

Description

MHS calibrated COMPASS Cell Based tools and libraries on CMOS 0.6µm process, bringing an additional option to its customer base to make designs where :

- the designer skill doesn't need to be as high as for full custom designs,
- the density and the speed are close to those of a full custom, while keeping a design cycle close to Composite Array one.

Features

- Calibrated on 3 ML, 0.6 µm drawn CMOS technology
- Set of libraries qualified on COMPASS tools
  - MHSC673 symbolic standard cell library
  - MHCC6DP1 datapath compiler
  - MHCC650 synchronous RAM & ROM compilers
  - MHCC62P1 two port RAM & FIFO compiler
  - MHCC6RA3 asynchronous RAM compiler
- Compared to 0.8 µm COMPASS libraries :
  - the density is improved by a factor better than 4
  - the speed is improved by 40 %
- MHS designed blocks can be imported
- Can be used for MGM1 blocks compilation
- Addresses designs when :
  - either speed & density are of essence
  - or quantity to be produced allows to amortize NRE
  - or for existing competition designs conversion
  - design modes : 1 or 5

Performances

The compilers can generate the following maximum size functions:

- asynchronous SRAMs from 128 to 64 Kbits with :
  - width ranging from 8 to 32 bits,
  - depth ranging from 16 to 2048 words.
- synchronous SRAM from 512 to 16K bits with :
  - width ranging from 8 to 32 bits,
  - depth ranging from 64 to 2048 words
- two port RAM from 128 to 32K bits with :
  - width ranging from 2 to 32 bits in 2 bit increments,
  - depth ranging from 64 to 2048 words.
- ROM from 256 to 128K bits with :
  - width ranging from 4 to 64 bits in 1 bit increment,
  - depth ranging from 64 to 4096 words.

The typical performances achieved are demonstrated in the following table, for some basic functions :

	Address access time (ns)	**Power consumption (mW/MHz)**	**Size (mm^2)**
2Kx16 two port RAM	12,8	10,76	11
4Kx32 ROM	21,5	11,12	2,5
2Kx8 synchronous RAM	17,2	2,76	2,5
2Kx32 asynchronous RAM	10,4	2,4	13

The package offering is similar to MG1M one.

Cell Based

CB8 0.8µm CMOS Cell-Based Designs

Description

MHS calibrated COMPASS Cell Based tools and libraries on CMOS 0.8µm, bringing an additional option to its customer base to make designs where :

- the designer skill doesn't need to be as high as for full custom designs,
- the density and the speed are close to those of a full custom, while keeping a design cycle close to the composite array one.

Features

- Calibrated on advance very low power CMOS process :
  - 2 metal layers
  - 0.8 µm effective channel length for N & P transistors
  - 12 µm epi wafers
- MHSC3xx set of libraries qualified on COMPASS tools :
  - VSC370 for standard cell, density optimized
  - VSC350 for standard cell, speed optimized
  - VDP300 for datapath compilation
  - VCC300 for logic compilation
- Design modes : 1 or 5

The package offering is similar to MCM one.

Cell Base Packaging Availability

PINCount	Package Type									
	Side Brazed	CerDip	PDIL	SO	LCC	PLCC (J)	CQFP (J) (*)	CQFP (L) (*)	PQFP (L)	PGA
14	●	●	●	●						
16	●	●	●	●						
18	●	●	●	●						
20	●	●	●	●		●				
24	●	●	●	●		●				
28	●	●	●	●	●	●				
40	●	●								
44					●	●	●		●	
48	●	●								
52						●			●	
64	●									
68					●	●	●			●
80								●	●	
84					●	●	●			●
100								●	●	●
120										●
128								●	●	
132								●		●
144										●
160								●	●	
176										●
196								●		
208									●	
209										●
240									C	
256										●
304									C	
323										C

C = Check for availability
(*) Consult factory for RT version – MQFL package is preferred

Digital Integration

Design Flows

Design Offering

Five different ASIC design offerings are available : ULC, Gate Arrays, Composite Arrays, Cell Based and Full Custom, each physical implementation giving an answer to the compromise : flexibility/unit price and integration/development cost.

Design Modes

Three different design modes can be agreed between Customer and MHS, depending on system and integration skills requirements.

Mode	Logic Design	Physical Layout	Design Tools
Customer Design	Customer	Customer	Customer tools
Customer and TEMIC Design	Customer	MHS	MHS supported tools (Netlist and simulation)
TEMIC Design	MHS	MHS	MHS supported tools (Netlist and simulation)

Supported tools are currently CADENCE, COMPASS, MENTOR, SYNOPSYS and VHDL/VITAL.

Design Modes versus Design Offering

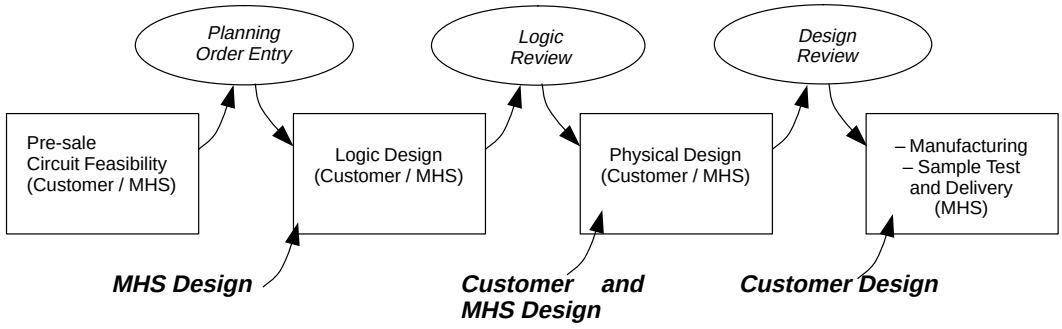
Offering \ Mode	Customer Design	Customer and MHS Design	MHS Design
ULC			□
Gate Array		x	□
Composite Array		x	□
Cell Based	x	○	□
Full Custom	x		

x : standard offer.
○ : depending on human and hardware ressources needed and/or available.
□ : specific development using MHS own expertise.

Design Phases and Meetings

The design of a circuit is separated into four main phases, separated by three major meetings between MHS and the Customer, as shown in Figure 1.

Figure 1. The design phases and meetings.



Processes

Description

MHS develops a wide range of CMOS processes, used for catalog products or ASICs' volume production. Their common features are high performance / high speed both with low power consumption, either in stand–by or operating modes.

MHS/TEMIC makes those processes available for selected customers/partners for their own design.

Features

	Technology	Well	Lithography (µm)	Poly Layers	Metal Layers	Operating Voltage (VO)	Characteristics
Digital Series							
FCC1D	CMOS	N	0.8	1	2	5 or 3	
FCC1S	CMOS	N	0.8	1	1	5 or 3	
FCC2D	CMOS	Twin	0.6	1	2	5 and/or 3	
FCC2T	CMOS	Twin	0.6	1	3	5 and/or 3	
FCB1D	BICMOS	Twin	0.8	1	2	5 and/or 3	NPN
Mixed Analog / Digital Series							
FCA1D FCA2D (1) FCA2T (2)	CMOS CMOS CMOS	N N	0.8 0.6 0.6	2 2 2	2 2 3	5 and/or 3 5 and/or 3 5 and/or 3	Low V_t
Non Volatile Series							
FCN1D FCN2D (1) FCN2T (2)	CMOS CMOS CMOS	2 2 2	0.8 0.6 0.6	1 1 1	2 2 3	5 5 and/or 3 5 and/or 3	EPROM EPROM
Radiation Tolerant Series							
FCT1D FCBTD FCT2D	CMOS BICMOS CMOS	N Twin Twin	0.8 0.8 0.6	1 1 1	2 2 3	5 5 5 and/or 3	Guard Ring Guard Ring Guard Ring

(1) Under Development (2) Planned

MHS Processes include digital CMOS processes and several derivatives done from the CMOS core basis :

- mixed analog/digital series with one more polysilicon layer and low V_t transistors
- non volatile series with high voltage NMOS transistors and programming/sensing/erasing capabilities
- radiation tolerant process with specific guard rings